# Ibraheem El Sheikha

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## Education

**University of Toronto** **Sept. 2023 – Apr. 2028**
*B.A.Sc. Computer Engineering, PEY Co-op* *Toronto, ON*

- **Top 30 ECE Student** out of ∼450 students (2025–2026) · **Dean's Honours List** (2023–2026) · **J. Edgar McAllister Research Fellowship**, 1 of 2 recipients across all 1st–3rd year ECE applicants (2025)

## Skills

- **Languages:** C++, C, Embedded C, Python, Verilog, RISC-V Assembly, Tcl, Bash
- **Hardware & Embedded:** RTL design, logic synthesis, computer architecture, FPGA design flows, STM32, UART/SPI/I2C
- **Tools:** Quartus Prime, ModelSim, OneSpin, Git, Linux, Docker, Flask, Jira, Confluence
- **Professional Skills:** Communication, leadership, organization, agile project management, teamwork, problem-solving

## Experience

**FPGA Software Engineering Intern** **May 2026 – Present**
*Microchip Technology | 16-month PEY* *Toronto, ON*

- Develop and migrate core **C++** functionality in the **synthesis** stage of internal FPGA design flows, moving legacy code paths onto modernized implementations.
- Debug interoperability failures between third-party **EDA** libraries and internal tooling, tracing root causes through **multi-million-line Verilog netlists** spanning DSP blocks, inferred memories, and multiple clock domains.
- Build **Python** netlist post-processing utilities and automated **Bash/Tcl** test infrastructure validating end-to-end design flows across benchmark designs.

**Undergraduate Researcher** **May 2025 – June 2026**
*University of Toronto ECE | Supervised by Prof. Salma Emara* *Toronto, ON*

- Built the hybrid retrieval pipeline behind **PiazzaPlus**, a published **Chrome extension**: **BM25** prefilters, then cosine similarity over **OpenAI embeddings** in **ChromaDB** reranks, served via a **Flask** API.
- Designed and ran evaluation against Piazza's native search, improving **MAP by 102.5%**, **MRR by 143.5%**, and **P@3 by 72.4%**.
- Captioned post images with a **vision model** and added them to the index, making diagrams and screenshots searchable with text.

## Projects

**Varphi CPU** | *Verilog, ModelSim, Computer Architecture* **July 2026 – Present**

- Designing a configurable **finite state machine processor** that executes a Turing machine description language directly in hardware, with **no program counter and no ALU**.
- Built a **Harvard datapath** whose transition-rule ROM is addressed by state plus each tape's read symbol, parameterized over tape count with **generate blocks** so one source elaborates to single- or multi-tape.
- Wrote per-module and top-level **testbenches** plus a **Python** visualizer that animates tape head movement from simulation logs.

**STM32 Perimeter Defense System** | *Embedded C, STM32, ESP32, Python* **Mar. 2026 – Apr. 2026**

- Built the sweep and ranging subsystem of a team radar turret: a stepper sweeps **360°** at 1/8 microstepping, firing an ultrasonic ping every 20 microsteps for **4.5°** resolution.
- Streamed polar contacts over **UART** at 115200 baud to a **Matplotlib** radar display, with status on an **SSD1306 OLED over I2C**.
- Integrated **identify-friend-or-foe** over an IR link, with an **ESP32** transmitting coded pulse frames classified after a 50 ms quiet gap.

**Embedded C Reversi** | *Embedded C, RISC-V, DE1-SoC FPGA* **Mar. 2025 – Apr. 2025**

- Built a two-player Reversi game in **embedded C** on a **RISC-V soft processor**, driving VGA and a PS/2 mouse through **memory-mapped I/O**.
- Implemented **double-buffered rendering** with vertical-sync polling off the VGA status register for a tear-free **60 Hz**.
- Decoded **PS/2 mouse packets** from the data register's RVALID field and wrote the game logic: move validation, directional tile flipping, score rendering, and win detection.

**Custom RISC-V CPU** | *Verilog, Quartus Prime, ModelSim* **Oct. 2024 – Dec. 2024**

- Implemented a **RISC-V-inspired CPU from scratch**: register file, **ALU**, sign-extension unit, controller FSM, datapath muxing, and a memory controller over a 512x32 RAM.
- Designed the **VGA display interface** and the memory arbitration letting processor and display adapter share one RAM; verified against directed testbenches in **ModelSim**.
- Built the ALU to cover `addi, add, sub, xor, and, or, sw, lw, beq, bne`; synthesized in **Quartus Prime Lite**.

## Publications

**Work-in-Progress: PiazzaPlus–Enhancing Piazza Search with Semantic Matching** **June 2026**

- **First author** with Prof. Salma Emara.
- Presented at the **ASEE Annual Conference & Exposition** (4,000+ attendees), one of few undergraduate presenters.